UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,685	10/15/2003	Yoshiyuki Wada	2003_1405A	3411

513 7590 06/28/2005

WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,685	WADA ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,12 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-5* is/are allowed.

6)☒ Claim(s) *1,6, 7,12 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/01/05 has been entered. An action on the RCE follows.

2. The amendment filed on 06/01/2005 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobita et al. (US Pat. 2002/0058743) in view of Barton (US Pat. 5308980) and Takano et al. (US Pat. 6376907).

Regarding claim 1, Tobita et al. disclose a semiconductor device comprising:

- a semiconductor element (12 in Fig. 2) having a first/bottom surface bearing external terminals (not numerically referenced- see Fig. 2) formed thereon with respective bumps (see Fig. 2) for external connection and a second/top surface opposite the first surface, the external terminals being in a form of a bump/protrusion (see Fig. 2)
- a spreader plate/reinforcing plate (SP/RP-19 in Fig. 2) confronting the second/top surface, the SP/RP having an external shape being larger than that of the semiconductor element (see Fig. 2)
- a bonding layer of a resin polymer binder/adhesive (18 in Fig. 2) for bonding the second/top surface and the spreader/plate such that the semiconductor element is bonded to the SP/RP via the bonding laver, the resin/adhesive having properties such as thermal coefficient of expansion (TCE), viscosity, modulus of elasticity (MOE), etc. to provide/allow the desired flexibility/deformation of the device package and associated components including the semiconductor element
- the resin polymer binder/adhesive comprising fillers including carbon fiber/powder and inorganic material such as aluminum oxide/nitride, silicon nitride, metallized resin/polymer (sections 0022-0039), the fillers having a distribution/range of particle size and diameter (sections 0022-0039)
- the bonding layer having a thickness as low as 50 microns (section 0058), and

- the device being mounted on a printed circuit board (PCB-see11 in Fig. 2).

(Fig. 2; Fig. 1C/1D; sections 0064, 0021-0064).

Tobita et al. fail to teach:

a) a thickness of the semiconductor element being at most 100 microns, and

b) the bonding layer having a modulus of elasticity (MOE) of at most 10,000Mpa.

a) Barton teaches a bonded integrated circuit (IC) device having thermally enhanced performance where the IC chip is conventionally lapped to a thickness as low as about 1 mil or 25 microns (12 in Fig. 3A/3B; Col. 4, lines 1-5) to provide the desired composite thermal expansion coefficient (TEC) for the bonded package (Col. 3, line 40-Col. 4, line 40; Col. 4-6).

b) Takano et al. teach using a ball grid array device (Fig. 1A) having a chip being adhesively bonded to a cover plate (14 and 16 respectively in Fig. 1A) using an adhesive/resin (17 in Fig. 1A) where the adhesive/resin has a MOE of about 900Mpa to provide the desired warpage/stress reduction and improved bonding (see Table 2; Col. 5, line 40- Col. 7, line 13).

Furthermore, determination of parameters such as adhesive/bonding layer thickness, die thickness, bonding layer composition including type/size/shape of filler particles, bump diameter/spacing, etc. in chip packaging and interconnect technology is

a subject of routine experimentation and optimization to achieve the desired TEC, MOE, reduced thermal/mechanical stress, etc.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the thickness of the semiconductor element being at most 100 microns and the bonding layer having the MOE of at most 10,000Mpa to allow for the deformation of the semiconductor element as taught by Barton and Takano et al. so that the desired composite TEC can be achieved, the package weight can be reduced and the warpage/stress can be reduced in Tobita's device.

Regarding claim 25, Tobita et al., Barton and Takano et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Tobita et al. further teach the bonding layer/adhesive partially covering side edges of a plurality of electronic parts/semiconductor elements (see 13 and 16 respectively in Fig. 1D).

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobita et al. (US Pat. 2002/0058743), Barton (US Pat. 5308980) and Takano et al. (US Pat. 6376907) as applied to claim 1 above, and further in view of Distefano et al. (US Pat. 6255738).

Regarding claims 6 and 7, Tobita et al., Barton and Takano et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Tobita et al. teach the

bonding layer being 50 microns thick, but fail to teach the bonding layer containing a filler having a diameter generally equal to the thickness of the bonding layer and the filler is in contact with the second surface of the semiconductor element respectively.

Distefano et al. teach using an encapsulant composition/resin (52 in Fig. 1) for a device to provide desired stress reduction, bonding, thermal expansion coefficient (CTE) and device protection (Col. 1-5) where the encapsulant/resin comprises:

- a number of fillers including a first, second and third filler, (Col. 2, lines 31-40; Col. 5, line 40- Col. 7, line 25; Col. 10)
- the first through third fillers having different particle size/diameter and size distribution/range including the size/diameter of about 50 microns, 2 microns and 0.1 microns respectively (Col. 6, lines 23, 33 and 67 respectively), and
- the first filler having the largest particle size/diameter among the fillers and the second filler having smaller particle size/diameter than that of the first filler

(Fig. 1; Col. 1-10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to realize that the filler particle diameter of about 50 microns being equal to the thickness of the bonding layer would provide the filler being in contact with the second surface of the semiconductor element and the plate as taught by Distefano et al. so that the desired thermal and mechanical properties can be achieved in Takano et al., Barton and Tobita's device.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tobita et al. (US Pat. 2002/0058743), Barton (US Pat. 5308980) and Takano et al. (US Pat. 6376907) as applied to claim 1 above, and further in view of Inaba et al. (US Pat. 6387734).

Regarding claim 12, Tobita et al., Barton and Takano et al. teach substantially the entire claimed structure as applied to claim 1 above, except:

- the semiconductor element being provided with a re-wiring layer on the first surface having a surface electrode formed on the surface, and
- an internal electrode formed inside thereof where the internal electrode is in communication between said surface electrode and the terminal for external connection

Inaba et al. teach using a chip size package/CSP/IC element (see 4/1 in Fig. 3 and 4) having a configuration comprising:

- the IC element being provided with a re-wiring/rerouting layer on the first surface (6/2 in Fig. 3 and 4) having a surface electrode (see 8 in Fig. 3 and 4) formed on the surface, and
- an internal electrode (1a in Fig. 4) formed inside thereof where the internal electrode is in communication between the surface electrode and a

terminal/bump electrode formed on the surface electrode (see 10 in Fig. 4) for external connection

(Fig. 3 and 4; Col. 4-7).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor element being provided with the re-wiring layer on the first surface having a surface electrode formed on the surface and an internal electrode formed inside thereof where the internal electrode is in communication between the surface electrode and the terminal for external connection as taught by Inaba et al. so that the desired routing and electrode pad relocation can be achieved in Takano et al., Barton and Tobita's device.

7. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobita et al. (US Pat. 2002/0058743), Barton (US Pat. 5308980), Takano et al. (US Pat. 6376907) and Distefano et al. (US Pat. 6255738) as applied to claims 1 and 7 above, and further in view of Shikata et al. (US Pat. 6255376).

Regarding claims 23 and 24, Tobita et al., Barton, Takano et al. and Distefano et al. teach substantially the entire claimed structure as applied to claims 1, 7, 26 and 18 above, except a wt.% of the fillers including aggregate wt.% of the first and second fillers in the resin binder being at most 30 wt.%.

Shikata et al. teach a resin-bonded device (Fig. 2) having a variety of resin/filler compositions where the binder resin has a composition comprising 5 wt.% filler particles (Col. 8, line 37) to provide the desired thermal conductivity, mechanical strength, viscosity and uniformity (Col. 6-8; Col. 5-18). The filler particles further comprising a first and a second filler (see samples 20-22 in Table 1; Col. 18).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a wt.% of the fillers including aggregated wt.% of the first and second fillers in the resin binder being 30 wt.% or less as taught by Shikata et al. so that the desired thermal and mechanical properties for the adhesive/resin can be achieved in Distefano et al., Takano et al., Barton and Tobita's device.

Response to Arguments

8. Applicant's arguments filed on 12-14-04 have been fully considered but they are not persuasive.

A. Applicant contends that Tobita et al. do not teach the semiconductor element thickness or MOE as claimed to allow deformation of the semiconductor element.

However, as explained above, the combined teachings of Takano et al. and Barton is applied to achieve the desired level of mechanical stress, deformation, etc. by using the optimized values for the thickness of the semiconductor element and the MOE for the bonding layer.

Allowable Subject Matter

9. Claims 3-5 are allowed.

Reasons for Allowance

10. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations " a semiconductor element having a thickness of at most 100 microns, said semiconductor element having a first surface bearing a terminal for external connection and a second surface opposite said first surface" and "a plate confronting said second surface, and a bonding layer between said second surface and said plate such that said semiconductor element is bonded to said plate via said bonding layer, said bonding layer having a thickness within a range of from 25um to 200um, wherein said bonding layer contains filler functioning as a spacer between said semiconductor element and said plate so as-to provide said bonding layer with a predetermined thickness" in a bumped device to be mounted on a circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

06-23-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800